signal is set to be active high while for writing to a memory cell the second select signal is set to be active high. In the matrix configuration the first select signal can be considered to be a read-wordline signal and the second select signal can be considered to be a write-wordline signal. In such an embodiment the sense signal sensed on the select line can be considered to be a bitline signal.

The present invention will now be explained with reference to the drawings in which

Fig. 1 shows an embodiment of a memory cell according to the invention,

Fig. 2 shows the general layout of a memory device according to the invention,

Fig. 3 shows a part of the matrix layout shown in Fig. 2,

Fig. 4 shows the layout of a sense amplifier according to the invention,

Fig. 5 shows signal diagrams of the signals in the memory device according to the invention,

Fig. 6 shows the circuitry of a unit for generating a reference voltage,

Fig. 7 shows the circuitry of a unit for generating a bias voltage,

Fig. 8 shows the circuitry of an address decoder used in the memory device according to the invention and

Fig. 9 shows signal diagrams for reading and writing a memory cell according to the invention.

Fig. 1 shows a preferred embodiment of the circuitry of a memory cell 1 according to the present invention. It comprises two bridge transistors MN0, MN1 whose drains are connected together and whose sources are both connected to a ground voltage level. The first bridge transistor MN0 is controllable by a first select signal, in particular a read-select signal rsel provided on a read wordline RWL. The second bridge transistor MN1 is controllable by a second select signal, in particular a write-select signal wsel provided on a write-wordline WWL. The common drain connection of said transistors MN0, MN1, called sense node SN in the following, is connected to a first end of a silicided polysilicium fuse resistor R which is connected to a program line PL with its other end for providing a program signal progv for programming the memory cell 1.